

REMARKS

Claims 1-13 are canceled. Claims 15-16 are withdrawn. Claim 14 is currently under examination. The Office Action initially rejected claim 14 under 35 U.S.C. §102(e) as being anticipated by the cited portions of U.S. Patent No. 5,351,197 to Upton et al. (hereinafter "Upton").

35 U.S.C. §102(e) Rejection, Upton

The Office Action initially rejected claim 14 under 35 U.S.C. §102(b) as being anticipated by the cited portions of Upton. In the cited portions of Upton, the Upton reference teaches a worst case design in which vertical pitch and horizontal pitch are all made of equal dimension to match the dimensions of the largest cells. As a result, no optimization of features is taking place. Rather, de-optimization is taking place in order to accommodate the cells with the largest dimensions.

In contrast, claim 14 recites the use of a MACRO. A MACRO is referred to on page 3 of the specification at lines 22-23 as:

"A MACRO is a block of transistors which have been optimized to perform a specific function. In a MACRO, the layout of the individual transistors, their operating characteristics, and their interconnections may have all been matched to each other for optimum performance. Thus, typically a MACRO is constructed from different sizes of transistors, which are embedded into the standard cell array as shown in Figure 7."

Thus, it is clear that the cited portions of the 5,351,197 patent are not teaching the embedding of a MACRO because the 5,351,197 patent does not teach an optimized block of transistors that are constructed from different size transistors. Rather, the cited portion of the 5,351,197 patent

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PATENT

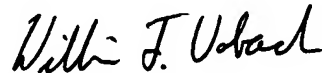
teaches the use of transistors that are sized and spaced the same without teaching any optimization. Furthermore, Fig. 7 of Applicant's disclosure shows cells of different width -- and thus optimized -- while the 5,351,197 patent teaches that the cells should have the same width. Consequently, the Applicant respectfully traverses the citation of the 5,351,197 since it has not been used to show the teaching of a MACRO embedded within a standard cell array. Therefore, the office action has not established a prima facie case of anticipation under 35 USC §102(e).

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,



William F. Vobach
Reg. No. 39,411

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 303-571-4000
Fax: 415-576-0300
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